**In the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Original) An electrically programmable and erasable memory device comprising:

a substrate of semiconductor material that includes a memory area and a peripheral area;

a memory cell formed in the memory area of the substrate, wherein the memory cell includes:

an electrically conductive floating gate disposed over and insulated from the substrate,

an electrically conductive control gate disposed adjacent to the floating gate, and

an insulating layer formed in the memory and peripheral areas that includes a first portion that is disposed between the control gate and the floating gate with a thickness permitting Fowler-Nordheim tunneling of charges therethrough; and

an MOS transistor formed in the peripheral area of the substrate, wherein the MOS transistor includes:

an electrically conductive poly gate disposed over and insulated from the substrate, and

a second portion of the insulating layer being disposed between the poly gate and the substrate and having a thickness that is greater than that of the first portion of the insulating layer;

wherein the first and second portions of the insulating layer being initially formed as a continuous layer of material.

2. (Original) The device of claim 1, wherein the memory cell further includes:

a first source region and a first drain region formed in the substrate, with a first channel region therebetween, wherein the floating gate is disposed over and insulated from at least a portion of the first channel region.

3. (Original) The device of claim 2, wherein the MOS transistor further includes:

a second source region and a second drain region formed in the substrate, with a second channel region therebetween, wherein the poly gate is disposed over and insulated from at least a portion of the second channel region.

4. (Original) The device of claim 1, wherein the control gate has a first portion that is disposed laterally adjacent to the floating gate.

5. (Original) The device of claim 4, wherein the control gate first portion is disposed over a portion of the first channel region.

6. (Original) The device of claim 5, wherein the control gate has a second portion that is disposed over the floating gate.

7. (Original) The device of claim 1, wherein:

the insulating layer second portion is formed directly on the peripheral area of the substrate, and the poly gate is formed directly on the insulating layer second portion.

8. (Original) The device of claim 7, wherein the insulating layer first portion further extends between the substrate and the control gate.

9. (Original) An electrically programmable and erasable memory device comprising:

a substrate of semiconductor material that includes a memory area and a peripheral area;

a memory cell formed in the memory area of the substrate, wherein the memory cell includes:

a first source region and a first drain region formed in the substrate, with a first channel region therebetween,

an electrically conductive floating gate disposed over and insulated from at least a portion of the first channel region,

an electrically conductive control gate disposed adjacent to the floating gate, and

an insulating layer formed in the memory and peripheral areas, wherein the insulating layer has a first portion that is disposed between the control gate and the floating gate with a thickness permitting Fowler-Nordheim tunneling of charges therethrough; and

an MOS transistor formed in the peripheral area of the substrate, wherein the MOS transistor includes:

a second source region and a second drain region formed in the substrate, with a second channel region therebetween,

an electrically conductive poly gate disposed over and insulated from at least a portion of the second channel region, and

a second portion of the insulating layer being disposed between the poly gate and the second channel region, wherein the second portion of the insulating layer has a thickness that is greater than that of the first portion of the insulating layer;

wherein the first and second portions of the insulating layer being initially formed as a continuous layer of material.

10. (Original) The device of claim 9, wherein the control gate has a first portion that is disposed laterally adjacent to the floating gate.

11. (Original) The device of claim 10, wherein the control gate first portion is disposed over a portion of the first channel region.

12. (Original) The device of claim 11, wherein the control gate has a second portion that is disposed over the floating gate.

13. (Original) The device of claim 9, wherein:

the insulating layer second portion is formed directly over the peripheral area of the substrate, and the poly gate is formed directly over the insulating layer second portion.

14. (Original) The device of claim 13, wherein the insulating layer first portion further extends between the substrate and the control gate.

Claims 15-27 (Previously cancelled)

28. (Previously added) The device of claim 1, wherein:

the insulating layer first portion is formed directly against the floating gate, and the control gate is formed directly on the insulating layer first portion; and

the insulating layer second portion is formed directly on the peripheral area of the substrate, and the poly gate is formed directly on the insulating layer second portion.

29. (Previously added) The device of claim 9, wherein:

the insulating layer first portion is formed directly against the floating gate, and the control gate is formed directly on the insulating layer first portion; and

the insulating layer second portion is formed directly on the peripheral area of the substrate, and the poly gate is formed directly on the insulating layer second portion.